

Substitute for form 1449A/PTO

FEB 2 8 2002

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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1

of

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Complete if Known

Application Number	09/956,903
Filing Date	September 21, 2001
First Named Inventor	FLETCHER, Thomas
Group Art Unit	2816 8124
Examiner Name	Not assigned Chat Do

Attorney Docket Number

2207/11270

U.S. PATENT DOCUMENTS

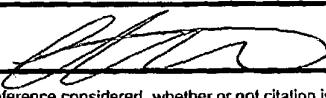
Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ³ (if known)			
CD		6,208,907 B1	03/27/2002	DURHAM et al	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
CD		Yee et al, "Clock-Delayed Domino for Dynamic Circuit Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 4, August 2000, pp 425-430	
CD		Yee et al, "Clock-Delayed Domino for Adder and Combinational Logic Design", IEEE, 1063-6404/96, pp 332-337, 1996	
CD		Jung, Perepelitsa, Sobelman, 'Time Borrowing in High-Speed Functional Units Using Skew-Tolerant Domino Circuits,' Proceedings, IEEE International Symposium on Circuits and Systems, pp. V-641 - V-644, 2000	
CD		Output Prediction Logic: A high performance CMOS Design Technique Presentation by Carl Sechen dated March 17, 2000.	
CD		Taub, Digital Circuits and Microprocessors, pages 205-212, McGraw-Hill, 1982	

Examiner Signature		Date Considered	8/21/04
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OCT 18 2001
JOHN C. FLETCHER
EXAMINER

U.S. PATENT DOCUMENTS				
Examiner Initials *	Cite No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
CD		5,777,491	07/07/98	Hwang
CD		4,570,084	02/11/86	Griffin et al
CD		5,977,789	11/02/99	Gayles
CD		5,568,069	10/22/96	Chow
CD		6,028,454	02/22/00	Elmasry et al

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Examiner Initials *	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		JP 5-259893 - Furuki (Abstract JP405-259893A)	10/8/93	Furuki		

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CD		Related U.S. Patent Application Serial No. 10/020,447, filed December 18, 2001	
CD		Related U.S. Patent Application Serial No. 09/892,565, filed June 28, 2001	
CD		Related U.S. Patent Application Serial No. 09/893,868, filed June 29, 2001	

Examiner Signature

Date Considered

8/21/04

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